ABSTRACT

A source synchronous clocking synchronizes data and clock signals transmitted between an ATM layer and a link layer. The source synchronous clocking includes a source clock domain in a first layer which includes a register having a first input for receiving a data signal, a second input for receiving a clock signal, and an output; and a buffer having an input for receiving the clock signal and an output, the buffer generating a delay that is substantially equivalent to a delay through the register. The source synchronous clocking further includes a destination clock domain in a second layer which includes a register having a first input and a second input, the first input of the register of the destination clock domain being coupled to the output of the register in the source clock domain.